

ISSUE CLASSIFICATION	
Class	Subclass

PATIENT NUMBER

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U.S. UTILITY Patent Application

12W O.I.P.E. SCANNED <u>2853</u> D.A. <u>LA</u>	PATENT DATE
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APPLICATION NO. 09/769953	CONT/PRIOR	CLASS 706-714	SUBCLASS 42	ART UNIT 2122 -32114	EXAMINER Bogachuk
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APPLICANTS

Sompong Olarig

TIME

Computer system having configurable core logic chipset for connection to a fault-tolerant accelerated graphics port bus and peripheral component interconnect bus

PTO-2040
12/99[illegible]

<input checked="" type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS. <div> <div>Sheets Drwg.</div> <div>Figs. Drwg.</div> <div>Print Fig.</div> </div>		CLAIMS ALLOWED <div> <div>Total Claims:</div> <div>Print Claim for O.G.</div> </div>	
	<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed. <input checked="" type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent No. <u>6,018,810</u>		NOTICE OF ALLOWANCE MAILED ISSUE FEE <div> <div>Amount Due</div> <div>Date Paid</div> </div>	
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